Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please cancel claims 13, 19, and 31. Please amend claims 12, 18, and 30, and add new claims 43-72, as follows:

Listing of Claims:

1-11. (Cancelled)

12. (Currently amended) A static content addressable memory array for a content addressable memory (CAM) device, comprising:

a plurality of word lines;

a plurality of data lines;

a latch having complementary data nodes capacitively coupled to ground;

first and second access transistors, each having a gate coupled to one of the plurality of word lines and coupled between a data node of the latch and a respective data line of the plurality; and

a match circuit coupled to one of the complementary data nodes of the latch, the match circuit including first and second transistors coupled in series between the data lines to which the first and second access transistors are coupled, the first transistor having a gate coupled to a first one of the data nodes and the second transistor having a gate coupled to a second one of the complementary data nodes, and further including a discharge transistor coupled between a match line and ground, and having a gate coupled to a node between the first and second transistors, the match circuit configured to discharge the ~~discharging a~~ match line in response to a data value stored at the data node to which the match circuit is coupled and compare data present on the respective data line mismatching.

13. (Cancelled)

14. (Original) The static CAM array of claim 12 wherein the latch is a first latch, the match circuit is a first match circuit, and the static CAM array further comprises:

a second latch having complementary data nodes capacitively coupled to ground, the first and second latches representing a single CAM memory cell;

third and fourth access transistors, each having a gate coupled to the word line to which the first and second access transistors are coupled, the third and fourth access transistors coupled between a data node of the second latch and a respective data line of the plurality; and

a second match circuit coupled to one of the complementary data nodes of the second latch, the match circuit discharging the match line in response to a data value stored at the data node to which the second match circuit is coupled and compare data present on the respective data line mismatching.

15. (Original) The static CAM array of claim 14 wherein the first and second match circuits comprise first and second switches, each switch having a control node and first and second nodes, the first switch having its first node coupled to ground and its second node 19.

coupled to the match line, and the second switch having its first node coupled to the first data line, its second terminal coupled to the control terminal of the first switch, and its control node coupled to the first data node.

16. (Original) The static CAM array of claim 14 wherein the first and second match circuits comprise first and second switches, each switch having a control node and first and second nodes, the first switch having its control terminal coupled to the first data node and its first node coupled to ground, the second switch having its control terminal coupled to the first data line, its first node coupled to the match line, and its second node coupled to the second node of the first transistor.

17. (Original) The static CAM array of claim 12 wherein the latch comprises:

a first switch having a first node coupled to a first of the complementary data nodes, a second node coupled to ground, and a control node coupled to the second data node;

a second switch having a first node coupled to the second data node, a second node coupled to ground, and a control node coupled to the first data node; and

first and second resistors, each resistor having a first terminal coupled to the power supply and a second terminal coupled to a respective data node.

18. (Currently amended) A content addressable memory (CAM) device, comprising:

an address bus;

a control bus;

a data bus;

an address decoder coupled to the address bus;

a read/write circuit coupled to the data bus; and

an array of CAM memory cells coupled to the address decoder, control circuit, and read/write circuit, the array comprising:

a plurality of word lines;

a plurality of data lines;

a latch having complementary data nodes capacitively coupled to ground;

first and second access transistors, each having a gate coupled to one of the plurality of word lines and coupled between a data node of the latch and a respective data line of the plurality; and

a match circuit coupled to one of the complementary data nodes of the latch, the match circuit <u>including first and second transistors coupled in series between the data lines to which the first and second access transistors are coupled, the first transistor having a gate coupled to a first one of the data nodes and the second transistor having a gate coupled to a second one of the complementary data nodes, and further including a discharge transistor coupled between a match line and ground, and having a gate coupled to a node between the first</u>

and second transistors, the match circuit configured to discharge the ~~discharging a~~ match line in response to a data value stored at the data node to which the match circuit is coupled and compare data present on the respective data line mismatching.

19. (Cancelled)

20. (Original) The CAM device of claim 18 wherein the latch of the array of CAM memory cells is a first latch, the match circuit is a first match circuit, and the static CAM array further comprises:

a second latch having complementary data nodes capacitively coupled to ground, the first and second latches representing a single CAM memory cell;

third and fourth access transistors, each having a gate coupled to the word line to which the first and second access transistors are coupled, the third and fourth access transistors coupled between a data node of the second latch and a respective data line of the plurality; and

a second match circuit coupled to one of the complementary data nodes of the second latch, the match circuit discharging the match line in response to a data value stored at the data node to which the second match circuit is coupled and compare data present on the respective data line mismatching.

21. (Original) The CAM device of claim 20 wherein the first and second match circuits of the array of CAM memory cells comprise first and second switches, each switch having a control node and first and second nodes, the first switch having its first node coupled to ground and its second node coupled to the match line, and the second switch having its first node coupled to the first data line, its second terminal coupled to the control terminal of the first switch, and its control node coupled to the first data node.

22. (Original) The CAM device of claim 20 wherein the first and second match circuits of the array of CAM memory cells comprise first and second switches, each switch having a control node and first and second nodes, the first switch having its control

terminal coupled to the first data node and its first node coupled to ground, the second switch having its control terminal coupled to the first data line, its first node coupled to the match line, and its second node coupled to the second node of the first transistor.

23. (Original) The CAM device of claim 18 wherein the latch of the array of CAM memory cells comprises:

a first switch having a first node coupled to a first of the complementary data nodes, a second node coupled to ground, and a control node coupled to the second data node;

a second switch having a first node coupled to the second data node, a second node coupled to ground, and a control node coupled to the first data node; and

first and second resistors, each resistor having a first terminal coupled to the power supply and a second terminal coupled to a respective data node.

24-29. (Cancelled)

30. (Currently amended) A computer system, comprising:

a data input device;

a data output device;

a processor coupled to the data input and output devices; and

a content addressable memory (CAM) device coupled to the processor, the CAM device comprising:

an address bus;

a control bus;

a data bus;

an address decoder coupled to the address bus;

a read/write circuit coupled to the data bus; and

an array of CAM memory cells coupled to the address decoder, control circuit, and read/write circuit, the array comprising:

a plurality of word lines;

a plurality of data lines;

a latch having complementary data nodes capacitively coupled to ground;

first and second access transistors, each having a gate coupled to one of the plurality of word lines and coupled between a data node of the latch and a respective data line of the plurality; and

a match circuit coupled to one of the complementary data nodes of the latch, the match circuit including first and second transistors coupled in series between the data lines to which the first and second access transistors are coupled, the first transistor having a gate coupled to a first one of the data nodes and the second transistor having a gate coupled to a second one of the complementary data nodes, and further including a discharge transistor coupled between a match line and ground, and having a gate coupled to a node between the first and second transistors, the match circuit configured to discharge the ~~discharging a~~ match line in response to a data value stored at the data node to which the match circuit is coupled and compare data present on the respective data line mismatching.

31. (Cancelled)

32. (Original) The computer system of claim 30 wherein the latch of the array of CAM memory cells is a first latch, the match circuit is a first match circuit, and the static CAM array further comprises:

a second latch having complementary data nodes capacitively coupled to ground, the first and second latches representing a single CAM memory cell;

third and fourth access transistors, each having a gate coupled to the word line to which the first and second access transistors are coupled, the third and fourth access transistors coupled between a data node of the second latch and a respective data line of the plurality; and

a second match circuit coupled to one of the complementary data nodes of the second latch, the match circuit discharging the match line in response to a data value stored at the

data node to which the second match circuit is coupled and compare data present on the respective data line mismatching.

33. (Original) The computer system of claim 32 wherein the first and second match circuits of the array of CAM memory cells comprise first and second switches, each switch having a control node and first and second nodes, the first switch having its first node coupled to ground and its second node coupled to the match line, and the second switch having its first node coupled to the first data line, its second terminal coupled to the control terminal of the first switch, and its control node coupled to the first data node.

34. (Original) The computer system of claim 32 wherein the first and second match circuits of the array of CAM memory cells comprise first and second switches, each switch having a control node and first and second nodes, the first switch having its control terminal coupled to the first data node and its first node coupled to ground, the second switch having its control terminal coupled to the first data line, its first node coupled to the match line, and its second node coupled to the second node of the first transistor.

35. (Original) The computer system of claim 30 wherein the latch of the array of CAM memory cells comprises:

a first switch having a first node coupled to a first of the complementary data nodes, a second node coupled to ground, and a control node coupled to the second data node;

a second switch having a first node coupled to the second data node, a second node coupled to ground, and a control node coupled to the first data node; and

first and second resistors, each resistor having a first terminal coupled to the power supply and a second terminal coupled to a respective data node.

36-42. (Cancelled)

43. (New) A static content addressable memory array for a content addressable memory (CAM) device, comprising:

a plurality of word lines;

a plurality of data lines;

a first latch having complementary data nodes capacitively coupled to ground;

a second latch having complementary data nodes capacitively coupled to ground, the first and second latches representing a single CAM memory cell;

first and second access transistors, each having a gate coupled to one of the plurality of word lines and coupled between a respective complementary data node of the first latch and a respective data line of the plurality;

third and fourth access transistors, each having a gate coupled to the word line to which the first and second access transistors are coupled, the third and fourth access transistors coupled between a respective complementary data node of the second latch and a respective data line of the plurality;

a first match circuit coupled to one of the complementary data nodes of the first latch, the first match circuit configured to discharge a match line in response to a data value stored at the complementary data node to which the first match circuit is coupled and compare data present on the respective data line mismatching; and

a second match circuit coupled to one of the complementary data nodes of the second latch, the second match circuit configured to discharge the match line in response to a data value stored at the complementary data node to which the second match circuit is coupled and compare data present on the respective data line mismatching.

44. (New) The static CAM array of claim 43 wherein the first match circuit comprises:

first and second transistors coupled in series between the data lines to which the first and second access transistors are coupled, the first transistor having a gate coupled to a first one of the complementary data nodes of the first latch and the second transistor having a gate coupled to a second one of the complementary data nodes of the first latch; and

a discharge transistor coupled between the match line and ground, and having a gate coupled to a node between the first and second transistors.

45. (New) The static CAM array of claim 43 wherein the first and second match circuits comprise first and second switches, each switch having a control node and first and second nodes, the first switch having its first node coupled to ground and its second node coupled to the match line, and the second switch having its first node coupled to the first data line, its second terminal coupled to the control terminal of the first switch, and its control node coupled to the one complementary data node of the respective latch.

46. (New) The static CAM array of claim 43 wherein the first and second match circuits comprise first and second switches, each switch having a control node and first and second nodes, the first switch having its control terminal coupled to the first data node and its first node coupled to ground, the second switch having its control terminal coupled to the first data line, its first node coupled to the match line, and its second node coupled to the second node of the first transistor.

47. (New) The static CAM array of claim 43 wherein the first latch comprises:

a first switch having a first node coupled to a first data node of the complementary data nodes of the first latch, a second node coupled to ground, and a control node coupled to a second data node of the complementary data nodes of the first latch;

a second switch having a first node coupled to the second data node of the first latch, a second node coupled to ground, and a control node coupled to the first data node of the first latch; and

first and second resistors, each resistor having a first terminal coupled to the power supply and a second terminal coupled to a respective complementary data node of the first latch.

48. (New) A static content addressable memory array for a content addressable memory (CAM) device, comprising:

a plurality of word lines;

a plurality of data lines;

a latch having complementary data nodes capacitively coupled to ground, the latch including a first switch, a second switch, and first and second resistors, the first switch having a first node coupled to a first data node of the complementary data nodes, a second node coupled to ground, and a control node coupled to a second data node of the complementary data nodes, the second switch having a first node coupled to the second data node, a second node coupled to ground, and a control node coupled to the first data node, and the first and second resistors each having a first terminal coupled to a power supply and a second terminal coupled to a respective data node;

first and second access transistors, each having a gate coupled to one of the plurality of word lines and coupled between a respective complementary data node of the latch and a respective data line of the plurality; and

a match circuit coupled to one of the complementary data nodes of the latch, the match circuit discharging a match line in response to a data value stored at the complementary data node to which the match circuit is coupled and compare data present on the respective data line mismatching.

49. (New) The static CAM array of claim 48 wherein the match circuit comprises:

first and second transistors coupled in series between the data lines to which the first and second access transistors are coupled, the first transistor having a gate coupled to a first one of the complementary data nodes and the second transistor having a gate coupled to a second one of the complementary data nodes; and

a discharge transistor coupled between the match line and ground, and having a gate coupled to a node between the first and second transistors.

50. (New) The static CAM array of claim 48 wherein the latch is a first latch, the match circuit is a first match circuit, and the static CAM array further comprises:

a second latch having complementary data nodes capacitively coupled to ground, the first and second latches representing a single CAM memory cell;

third and fourth access transistors, each having a gate coupled to the word line to which the first and second access transistors are coupled, the third and fourth access transistors coupled between a respective complementary data node of the second latch and a respective data line of the plurality; and

a second match circuit coupled to one of the complementary data nodes of the second latch, the match circuit discharging the match line in response to a data value stored at the complementary data node to which the second match circuit is coupled and compare data present on the respective data line mismatching.

51. (New) The static CAM array of claim 50 wherein the first and second match circuits comprise first and second switches, each switch having a control node and first and second nodes, the first switch having its first node coupled to ground and its second node coupled to the match line, and the second switch having its first node coupled to the first data line, its second terminal coupled to the control terminal of the first switch, and its control node coupled to the one complementary data node of the respective latch.

52. (New) The static CAM array of claim 50 wherein the first and second match circuits comprise first and second switches, each switch having a control node and first and second nodes, the first switch having its control terminal coupled to the first data node and its first node coupled to ground, the second switch having its control terminal coupled to the first data line, its first node coupled to the match line, and its second node coupled to the second node of the first transistor.

53. (New) A content addressable memory (CAM) device, comprising:

an address bus;

a control bus;

a data bus;

an address decoder coupled to the address bus;

a read/write circuit coupled to the data bus; and

an array of CAM cells coupled to the address decoder, control circuit, and read/write circuit, the array comprising:

a plurality of word lines;

a plurality of data lines;

a first latch having complementary data nodes capacitively coupled to ground;

a second latch having complementary data nodes capacitively coupled to ground, the first and second latches representing a single CAM memory cell;

first and second access transistors, each having a gate coupled to one of the plurality of word lines and coupled between a respective complementary data node of the first latch and a respective data line of the plurality;

third and fourth access transistors, each having a gate coupled to the word line to which the first and second access transistors are coupled, the third and fourth access transistors coupled between a respective complementary data node of the second latch and a respective data line of the plurality;

a first match circuit coupled to one of the complementary data nodes of the first latch, the first match circuit configured to discharge a match line in response to a data value stored at the complementary data node to which the first match circuit is coupled and compare data present on the respective data line mismatching; and

a second match circuit coupled to one of the complementary data nodes of the second latch, the second match circuit configured to discharge the match line in response to a data value stored at the complementary data node to which the second match circuit is coupled and compare data present on the respective data line mismatching.

54. (New) The CAM device of claim 53 wherein the first match circuit of the array of CAM cells comprises:

first and second transistors coupled in series between the data lines to which the first and second access transistors are coupled, the first transistor having a gate coupled to a first one of the complementary data nodes of the first latch and the second transistor having a gate coupled to a second one of the complementary data nodes of the first latch; and

a discharge transistor coupled between the match line and ground, and having a gate coupled to a node between the first and second transistors.

55. (New) The CAM device of claim 53 wherein the first and second match circuits of the array of CAM cells comprise first and second switches, each switch having a control node and first and second nodes, the first switch having its first node coupled to ground and its second node coupled to the match line, and the second switch having its first node coupled to the first data line, its second terminal coupled to the control terminal of the first switch, and its control node coupled to the one complementary data node of the respective latch.

56. (New) The CAM device of claim 53 wherein the first and second match circuits of the array of CAM cells comprise first and second switches, each switch having a control node and first and second nodes, the first switch having its control terminal coupled to the first data node and its first node coupled to ground, the second switch having its control terminal coupled to the first data line, its first node coupled to the match line, and its second node coupled to the second node of the first transistor.

57. (New) The CAM device of claim 53 wherein the first latch of the array of CAM cells comprises:

a first switch having a first node coupled to a first data node of the complementary data nodes of the first latch, a second node coupled to ground, and a control node coupled to a second data node of the complementary data nodes of the first latch;

a second switch having a first node coupled to the second data node of the first latch, a second node coupled to ground, and a control node coupled to the first data node of the first latch; and

first and second resistors, each resistor having a first terminal coupled to the power supply and a second terminal coupled to a respective data node of the first latch.

58. (New) A content addressable memory (CAM) device, comprising:

an address bus;

a control bus;

a data bus;

an address decoder coupled to the address bus;

a read/write circuit coupled to the data bus; and

an array of CAM cells coupled to the address decoder, control circuit, and read/write circuit, the array comprising:

a plurality of word lines;

a plurality of data lines;

a latch having complementary data nodes capacitively coupled to ground, the latch including a first switch, a second switch, and first and second resistors, the first switch having a first node coupled to a first data node of the complementary data nodes, a second node coupled to ground, and a control node coupled to a second data node of the complementary data nodes, the second switch having a first node coupled to the second data node, a second node coupled to ground, and a control node coupled to the first data node, and the first and second resistors each having a first terminal coupled to a power supply and a second terminal coupled to a respective data node;

first and second access transistors, each having a gate coupled to one of the plurality of word lines and coupled between a respective complementary data node of the latch and a respective data line of the plurality; and

a match circuit coupled to one of the complementary data nodes of the latch, the match circuit discharging a match line in response to a data value stored at the

complementary data node to which the match circuit is coupled and compare data present on the respective data line mismatching.

59. (New) The CAM device of claim 58 wherein the match circuit of the array of CAM cells comprises:

first and second transistors coupled in series between the data lines to which the first and second access transistors are coupled, the first transistor having a gate coupled to a first one of the complementary data nodes and the second transistor having a gate coupled to a second one of the complementary data nodes; and

a discharge transistor coupled between the match line and ground, and having a gate coupled to a node between the first and second transistors.

60. (New) The CAM device of claim 58 wherein the latch is a first latch, the match circuit is a first match circuit, and the static CAM array further comprises:

a second latch having complementary data nodes capacitively coupled to ground, the first and second latches representing a single CAM memory cell;

third and fourth access transistors, each having a gate coupled to the word line to which the first and second access transistors are coupled, the third and fourth access transistors coupled between a respective complementary data node of the second latch and a respective data line of the plurality; and

a second match circuit coupled to one of the complementary data nodes of the second latch, the match circuit discharging the match line in response to a data value stored at the complementary data node to which the second match circuit is coupled and compare data present on the respective data line mismatching.

61. (New) The CAM device of claim 60 wherein the first and second match circuits of the array of CAM cells comprise first and second switches, each switch having a control node and first and second nodes, the first switch having its first node coupled to ground and its second node coupled to the match line, and the second switch having its first node

coupled to the first data line, its second terminal coupled to the control terminal of the first switch, and its control node coupled to the one complementary data node of the respective latch.

62. (New) The CAM device of claim 60 wherein the first and second match circuits of the array of CAM cells comprise first and second switches, each switch having a control node and first and second nodes, the first switch having its control terminal coupled to the first data node and its first node coupled to ground, the second switch having its control terminal coupled to the first data line, its first node coupled to the match line, and its second node coupled to the second node of the first transistor.

63. (New) A computer system, comprising:

a data input device;

a data output device;

a processor coupled to the data input and output devices; and

a content addressable memory (CAM) device coupled to the processor, the CAM device comprising:

an address bus;

a control bus;

a data bus;

an address decoder coupled to the address bus;

a read/write circuit coupled to the data bus; and

an array of CAM cells coupled to the address decoder, control circuit, and read/write circuit, the array comprising:

a plurality of word lines;

a plurality of data lines;

a first latch having complementary data nodes capacitively coupled to ground;

a second latch having complementary data nodes capacitively coupled to ground, the first and second latches representing a single CAM memory cell;

first and second access transistors, each having a gate coupled to one of the plurality of word lines and coupled between a respective complementary data node of the first latch and a respective data line of the plurality;

third and fourth access transistors, each having a gate coupled to the word line to which the first and second access transistors are coupled, the third and fourth access transistors coupled between a respective complementary data node of the second latch and a respective data line of the plurality;

a first match circuit coupled to one of the complementary data nodes of the first latch, the first match circuit configured to discharge a match line in response to a data value stored at the complementary data node to which the first match circuit is coupled and compare data present on the respective data line mismatching; and

a second match circuit coupled to one of the complementary data nodes of the second latch, the second match circuit configured to discharge the match line in response to a data value stored at the complementary data node to which the second match circuit is coupled and compare data present on the respective data line mismatching.

64. (New) The computer system of claim 63 wherein the first match circuit of the array of CAM cells comprises:

first and second transistors coupled in series between the data lines to which the first and second access transistors are coupled, the first transistor having a gate coupled to a first one of the complementary data nodes of the first latch and the second transistor having a gate coupled to a second one of the complementary data nodes of the first latch; and

a discharge transistor coupled between the match line and ground, and having a gate coupled to a node between the first and second transistors.

65. (New) The computer system of claim 63 wherein the first and second match circuits of the array of CAM cells comprise first and second switches, each switch having a control node and first and second nodes, the first switch having its first node coupled to ground and its second node coupled to the match line, and the second switch having its first node

coupled to the first data line, its second terminal coupled to the control terminal of the first switch, and its control node coupled to the one complementary data node of the respective latch.

66. (New) The computer system of claim 63 wherein the first and second match circuits of the array of CAM cells comprise first and second switches, each switch having a control node and first and second nodes, the first switch having its control terminal coupled to the first data node and its first node coupled to ground, the second switch having its control terminal coupled to the first data line, its first node coupled to the match line, and its second node coupled to the second node of the first transistor.

67. (New) The computer system of claim 63 wherein the first latch of the array of CAM cells comprises:

a first switch having a first node coupled to a first data node of the complementary data nodes of the first latch, a second node coupled to ground, and a control node coupled to a second data node of the complementary data nodes of the first latch;

a second switch having a first node coupled to the second data node of the first latch, a second node coupled to ground, and a control node coupled to the first data node of the first latch; and

first and second resistors, each resistor having a first terminal coupled to the power supply and a second terminal coupled to a respective data node of the first latch.

68. (New) A computer system, comprising:

a data input device;

a data output device;

a processor coupled to the data input and output devices; and

a content addressable memory (CAM) device coupled to the processor, the CAM device comprising:

an address bus;

a control bus;

a data bus;

an address decoder coupled to the address bus;

a read/write circuit coupled to the data bus; and

an array of CAM cells coupled to the address decoder, control circuit, and read/write circuit, the array comprising:

a plurality of word lines;

a plurality of data lines;

a latch having complementary data nodes capacitively coupled to ground, the latch including a first switch, a second switch, and first and second resistors, the first switch having a first node coupled to a first data node of the complementary data nodes, a second node coupled to ground, and a control node coupled to a second data node of the complementary data nodes, the second switch having a first node coupled to the second data node, a second node coupled to ground, and a control node coupled to the first data node, and the first and second resistors each having a first terminal coupled to a power supply and a second terminal coupled to a respective data node;

first and second access transistors, each having a gate coupled to one of the plurality of word lines and coupled between a respective complementary data node of the latch and a respective data line of the plurality; and

a match circuit coupled to one of the complementary data nodes of the latch, the match circuit discharging a match line in response to a data value stored at the complementary data node to which the match circuit is coupled and compare data present on the respective data line mismatching.

69. (New) The computer system of claim 68 wherein the match circuit of the array of CAM cells comprises:

first and second transistors coupled in series between the data lines to which the first and second access transistors are coupled, the first transistor having a gate coupled to a first one of the complementary data nodes and the second transistor having a gate coupled to a second one of the complementary data nodes; and

a discharge transistor coupled between the match line and ground, and having a gate coupled to a node between the first and second transistors.

70. (New) The computer system of claim 68 wherein the latch is a first latch, the match circuit is a first match circuit, and the static CAM array further comprises:

a second latch having complementary data nodes capacitively coupled to ground, the first and second latches representing a single CAM memory cell;

third and fourth access transistors, each having a gate coupled to the word line to which the first and second access transistors are coupled, the third and fourth access transistors coupled between a respective complementary data node of the second latch and a respective data line of the plurality; and

a second match circuit coupled to one of the complementary data nodes of the second latch, the match circuit discharging the match line in response to a data value stored at the complementary data node to which the second match circuit is coupled and compare data present on the respective data line mismatching.

71. (New) The computer system of claim 68 wherein the first and second match circuits of the array of CAM cells comprise first and second switches, each switch having a control node and first and second nodes, the first switch having its first node coupled to ground and its second node coupled to the match line, and the second switch having its first node coupled to the first data line, its second terminal coupled to the control terminal of the first switch, and its control node coupled to the one complementary data node of the respective latch.

72. (New) The computer system of claim 70 wherein the first and second match circuits of the array of CAM cells comprise first and second switches, each switch having a control node and first and second nodes, the first switch having its control terminal coupled to the first data node and its first node coupled to ground, the second switch having its control terminal coupled to the first data line, its first node coupled to the match line, and its second node coupled to the second node of the first transistor.